Office Action Summary	Application No.	Applicant(s)	
	10/082,182	NARAZAKI ET AL.	
	Examin r	Art Unit	
	Leonard S Liang	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05/05/05 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The lengthy specification and drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification and drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 6-7, 11-13, 15, 17-18, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Harper et al (WO Pat 9100566).

Harper et al discloses:

- {claim 1} a CPU having plural modes (page 6, lines 1-11) including a mode to reduce the power consumption by suspending the clock signal as an operational mode (page 6, lines 18-37; page 7, lines 1-10); receiving signal from power switching means as NMI interrupt signal for the execution of NMI interrupt process (page 50, line 37 – page 51, line 21; page 34, line 34 – page 36, lines 15); non-volatile memory means; user logic circuit means; a mask signal generating portion; a gate circuit; control means (figure 3, 5; page 34, line 34 – page 36, line 15; page 50, line 37 – page 51, line 21; pages 36-39)

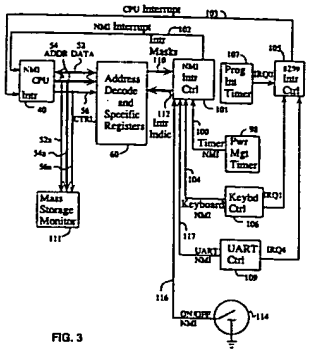
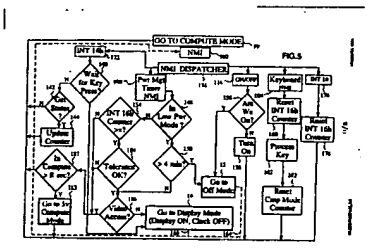


FIG. 3

- {claim 2} wherein if the flag is ON, the power supply OFF is operated as the operation to change the flag to OFF, and as the operational mode change of the CPU, the clock signal is suspended and the mode is changed to the one for reducing power consumption (figure 5, reference 156; page 51, lines 1-21)



- {claim 4} wherein if the flag is OFF, the power supply ON is operated as the operation to change the flag to ON, and as the operational mode change of the CPU, the clock signal is suspended and the mode is changed from the one for reducing the power consumption (figure 5, reference 156; page 51, lines 1-21)
- {claim 6} a CPU having plural modes; abnormality detection; user logic circuit means; a mask signal generating portion; a gate circuit; control means (figure 3-5; page 34, line 39 – page 36, line 15; page 50, line 35 – page 51, line 21; page 36-39)

- {claim 7} a second abnormality means, wherein the gate circuit further executes the logical operation of abnormal signal from the second abnormality detection means (naturally suggested in view of the trapping function disclosed on pages 36-39)
- {claim 11} a CPU having plural modes; user logic circuit means; a mask signal generating portion; a gate circuit; control means (figure 3-5; page 34, line 39 – page 36, line 15; page 50, line 35 – page 51, line 21; page 36-39)
- {claim 12} a CPU having plural modes; retaining a power supply status flag; outputting trigger signal; generating mask signal; operational process of computer (and ink jet recording apparatus by inference to computer) is executed in accordance with the flag retained in the flag retaining step when the NMI interrupt process is executed by signal from the power switching means, and the flag retained in the flag retaining process is updated in the trigger signal outputting step for outputting trigger signal in accordance with the setting for the user logic circuit, and mask signal is generated in the mask signal generating step in accordance with the trigger signal for making signal from the power switching means invalid by the generation of the mask signal until the operational process is completed (figure 3-5; page 34, line 39 – page 36, line 15; page 50, line 35 – page 51, line 21; page 36-39)
- {claim 13} if the flag is ON, the operation is an operational process of the power supply OFF, and the flag is changed to suspend the clock signal as the

operational mode change of the CPU for changing the mode to the one for reducing the power consumption (figure 5, reference 156; page 51, lines 1-21)

- {claim 15} if the flag is OFF, the operation is an operational process of the power supply ON, and the flag is changed to suspend the clock signal as the operational mode change of the CPU for changing the mode from the one for reducing the power consumption (figure 5, reference 156; page 51, lines 1-21)
- {claim 17} a CPU having plural modes; detecting abnormality; retaining a power supply status flag on non-volatile memory means; outputting trigger signal from user logic circuit means; generating mask signal; abnormality is detected in the abnormality detecting step (figure 3-5; page 34, line 39 – page 36, line 15; page 50, line 35 – page 51, line 21; page 36-39)
- {claim 18} a second abnormality step; the second abnormality detection means detects abnormality, and abnormality detection means outputs signal to the gate circuit (as taught in claim 7)
- {claim 22} a CPU having plural modes; deciding whether or not the NMI interrupt signal is inputted into the input means for a designated member; outputting trigger signal from user logic circuit means; generating mask signal in the NMI interrupt signal generating portion for the NMI interrupt by receiving the trigger signal, wherein the NMI interrupt prohibition is set for the user logic circuit means when the input of the NMI interrupt signal is made in the designated number in the determining step subsequent to the NMI interrupt process executed by the input of signal from the power switching means, the

trigger signal is output in the trigger signal generating step in accordance with the setting to user logic circuit means for generating mask signal in the mask signal generating step in accordance with the output of the trigger signal

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 5, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harper et al (WO Pat 9100566) in view of Kanbayashi et al (EP Pat 0782924 A1).

Harper et al discloses:

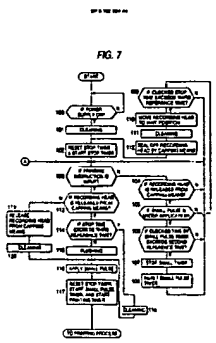
- {claims 3 and 5} an ink jet recording apparatus (as taught in claims 2 and 4)
- {claims 14 and 16} a method for controlling an ink jet recording apparatus (as taught in claims 13 and 15)

Harper et al differs from the claimed invention in that it does not disclose:

- {claims 3 and 14} the power supply OFF operation includes the capping operation to protect the recording head mounted on the ink jet recording apparatus
- {claims 5 and 16} the power supply ON operation includes the recovery operation for recovering the recording head mounted on the ink jet recording apparatus

Kanbayashi et al discloses:

- {claims 3 and 14} the power supply OFF operation includes the capping operation to protect the recording head mounted on the ink jet recording apparatus (figure 7, reference 112; column 6, line 59 – column 7, line 9)



- {claims 5 and 16} the power supply ON operation includes the recovery operation for recovering the recording head mounted on the ink jet recording apparatus (figure 7, reference 100, 101)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Kanbayashi et al into the invention of Harper et al. The motivation for the skilled artisan in doing so is to gain the benefit of performing capping in order to prevent nozzle openings from being clogged up (abstract).

4. Claims 8, 9, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harper et al (WO Pat 9100566) in view of Yoshimura et al (US Pat 5262872).

Harper et al discloses:

- {claims 8 and 9} an ink jet recording apparatus (as taught in claim 6)

- {claims 19 and 20} a method of controlling an ink jet recording apparatus (as taught in claim 17)

Harper et al differs from the claimed invention in that it does not disclose:

- {claim 8} the abnormality detection means detects the abnormal temperature rise of the recording head mounted on the ink jet recording apparatus
- {claim 9} the second abnormality detection means detects the excessive voltage of the power supply provided for the ink jet recording apparatus
- {claim 19} the abnormal temperature of the recording head mounted on the ink jet recording apparatus is detected in the abnormality detecting step
- {claim 20} the excessive voltage of the power supply provided for the ink jet recording apparatus is detected in the second abnormality step

Yoshimura et al discloses:

- {claim 8} the abnormality detection means detects the abnormal temperature rise of the recording head mounted on the ink jet recording apparatus (column 23, lines 41-67)
- {claim 9} the second abnormality detection means detects the excessive voltage of the power supply provided for the ink jet recording apparatus (column 27, lines 28-39)
- {claim 19} the abnormal temperature of the recording head mounted on the ink jet recording apparatus is detected in the abnormality detecting step (as taught in claim 8)

- {claim 20} the excessive voltage of the power supply provided for the ink jet recording apparatus is detected in the second abnormality step (as taught in claim 9)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Yoshimura et al into the invention of Harper et al. The motivation for the skilled artisan in doing so is to gain the benefit of being able to detect errors (abstract).

5. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harper et al (WO Pat 9100566) in view of Kaneko et al (US Pat 5428379).

Harper et al discloses, with respect to claims 10 and 21, an ink jet recording apparatus (ati 1) and a method for controlling an ink jet recording apparatus (as taught in claim 12).

Harper et al differs from the claimed invention in that it does not disclose that the recording head is provided with a plurality of recording members including an electrothermal converting element for generating thermal energy as energy for discharging ink.

Kaneko et al discloses, with respect to claims 10 and 21, the recording head is provided with a plurality of recording members including an electrothermal converting element for generating thermal energy as energy for discharging ink (column 3, lines 17-23).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the electrothermal converting element disclosed by Kaneko et al into the invention of Harper et al. The motivation for the skilled artisan in doing so is to gain the benefit of generating thermal energy as energy for discharging ink (column 3, lines 17-23).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Oida et al (US Pat 5581668) discloses a method and apparatus for processing data.

Masaki (US Pat 5652607) discloses a recording apparatus.

Yoda et al (US Pat 6511150) discloses an ink jet printer, an initialization control method therefor, and a data recording medium.

Takahashi (US Pat 6081663) discloses an information processing method and apparatus having a power-saving control feature.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonard S Liang whose telephone number is (703) 305-4754. The examiner can normally be reached on 8:30-5 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Russ Adams can be reached on (703) 308-2847. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

lsl LSL
May 5, 2003

JUDY NGUYEN
PRIMARY EXAMINER